Helix Semiconductors
HS200 EVB Manual

HS200 +48Vin 15W DC-DC MuxCapacitor™ Evaluation Board

The Helix Semiconductors HS200 DC-DC MuxCapacitor Evaluation Boards offer three configurations: Single 12V output, Triple 24V/12V/6V outputs, and a regulated 5V output. Each evaluation board is self contained and ready for use.

Wiring connection diagram, schematic and BOM for each board are included in this manual. Gerber files are available upon request.

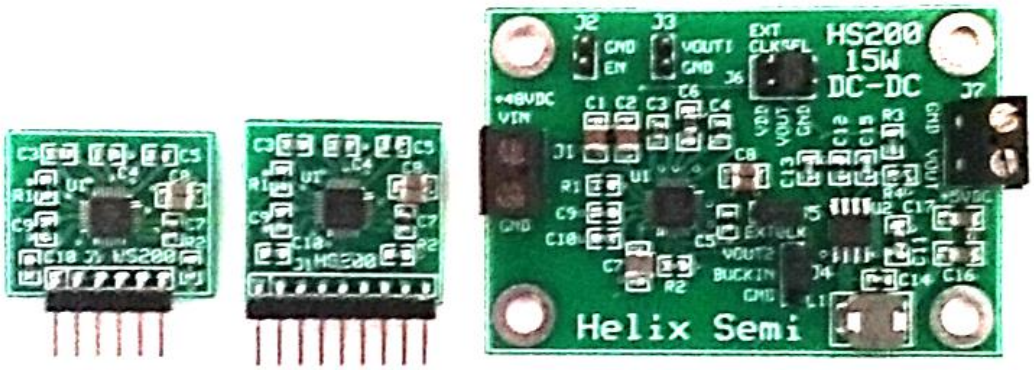
Applications

- Telecom Blades, Data Centers
- PoE: Wireless Access Points, Security Cameras, VoIP Phones
- Industrial Controllers, HVAC
- IoT & IIoT Gateways
- Electric & Hybrid Automobiles

Features

- Three Configurations
  - Single 12V Output
  - Triple 24V/12V/6V Outputs
  - Regulated 5V Output
- 15W Output (Multiple Outputs)
  - Pout = Pout1 + Pout2 + Pout3
- External Control Signals
  - Enable
  - External Clock Enable
  - External Clock Input
- Idle Operation: Active, No-Load
  - 0.5mW Power Consumption
  - Active On Output
- > 97% Efficiency @ 2.6W
- > 90% Efficiency @ 15W

HS200 Evaluation Boards



Single 12V Output Triple 24/12/6V Outputs Regulated 5V Output

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1 HS200 Single 12V Output EVB

The HS200 Single 12V Output EVB can be operated as a standalone Divide-By-4 voltage reducer (Figure 1) or synchronized with a SMPS (Figure 2).

When the HS200 is providing power to a SMPS, the synchronization feature of the HS200 allows the HS200 MuxCapacitor switching to slow down as the SMPS enters pulse skipping. This operation reduces switching power losses at no-load to light-load conditions. The EXTCLK can be provided by either a FET gate drive signal or a buck regulator's switched output. Both the EXTCLKSEL and EXTCLK inputs accept up to 30V signals.

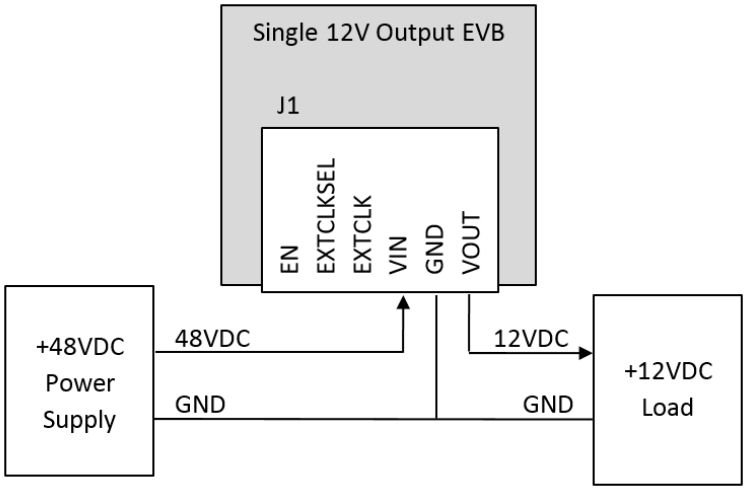

Figure 1: HS200 Single 12V Output EVB Standalone Wiring Diagram

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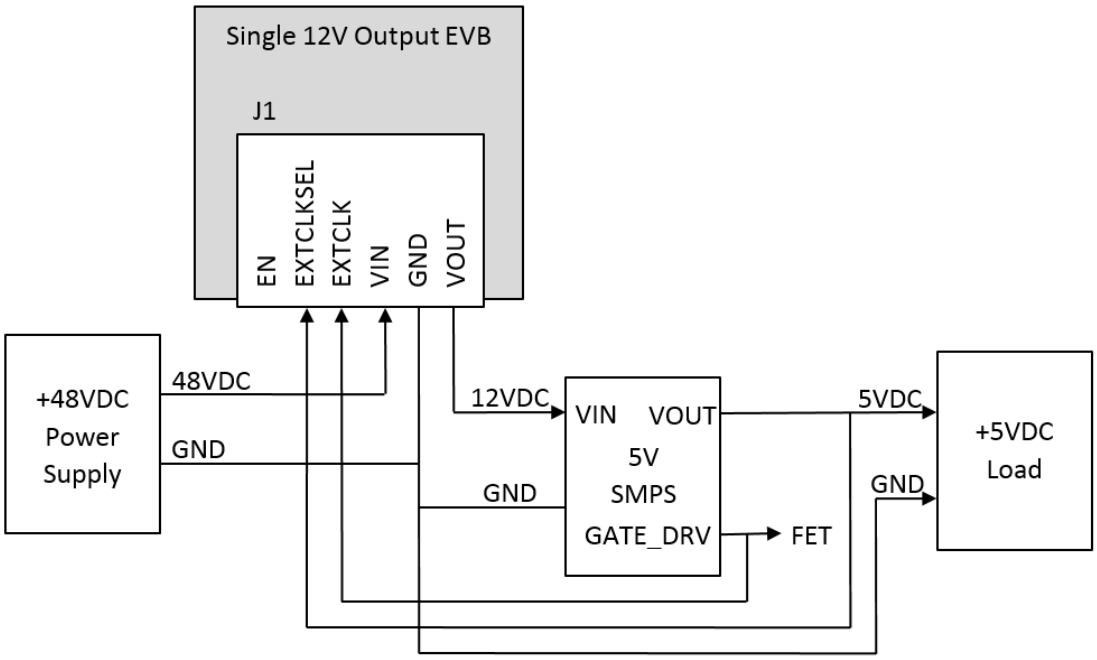

Figure 2: HS200 Single 12V Output EVB SMPS Wiring Diagram

Table 1: HS200 Single 12V Output EVB Connector – J1

Pin No.	Name	Description
1	EN	Device Enable: Input Pin, On-board 100KΩ Pull-Up, 60Vmax 0 = Disable, 1 = Enable
2	EXTCLKSEL	External Clock Sync Enable: Input Pin, Internal 2MΩ Pull-Down, 30Vmax 0 = Internal Clock, 1 = External Clock
3	EXTCLK	External Clock Sync: Input pin, Internal 2MΩ Pull-Down, 30Vmax
4	VIN	+48VDC Input Power Pin
5	GND	Power GND Pin
6	VOUT	15W +12VDC Output Power Pin

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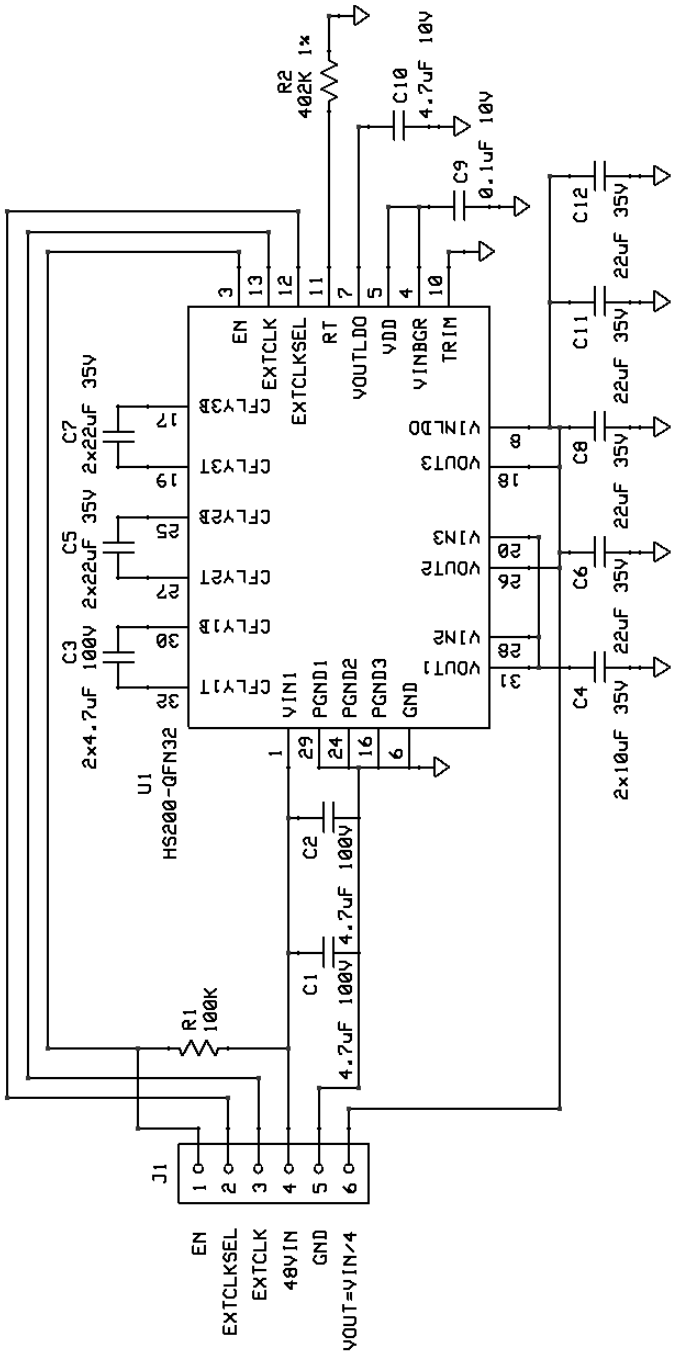

Figure 3: HS200 Single 12V Output EVB Schematic

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Table 2: HS200 Single 12V Output EVB Bill of Materials (BOM)

Qty	Ref. No.	Description	Package	Manufacturer
1	C9	CAP, 0.1µF±10%, 16V	CC0603	Murata GRM188R71C104KA01J
1	C10	CAP, 4.7µF±10%, 16V	CC0805	Murata GRM188C81C475KE11J
2	C4x2	CAP, 10µF±10%, 35V	CC0805	Murata GRM21BC8YA106KE11L
8	C5x2, C6, C7x2, C8, C11, C12	CAP, 22µF±10%, 35V	CC0805	TDK C2012X5R1V226M125AC
3	C1, C2, C3x2	CAP, 4.7µF±10%, 100V	CC1206	Murata GRJ32ER71K475KE11L
1	R1	RES, 100KΩ±10%	CC0603	Rohm ESR03EZPJ104
1	R2	RES, 402 KΩ±1%	CC0603	Rohm MCR03ERTF4023
1	U1	IC, HS200, QFN5x5, 32P 0.5	QFN32	Helix Semiconductors
1	J1	CONN, 6P, M, R/A, 0.100	SIP100P6	Hirose A2-6PA-2.54DS(71)

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2 HS200 Triple 24V/12V/6V Output EVB

The HS200 Triple 24V/12V/6V Output EVB can be operated as a standalone Divide-By-4 voltage reducer (Figure 4) or synchronized with a SMPS (Figure 5).

When the HS200 is providing power to a SMPS, the synchronization feature of the HS200 allows the HS200 MuxCapacitor switching to slow down as the SMPS enters pulse skipping. This operation reduces switching power losses at no-load to light-load conditions. The EXTCLK can be provided by either a FET gate drive signal or a buck regulator's switched output. Both the EXTCLKSEL and EXTCLK inputs accept up to 30V signals.

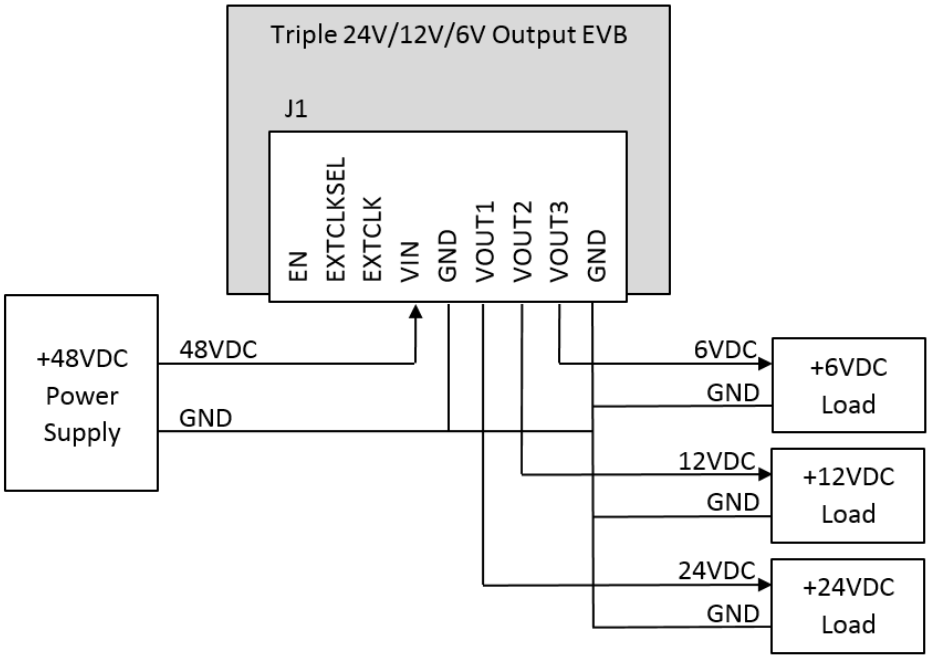

Figure 4: HS200 Triple 24V/12V/6V Output EVB Standalone Wiring Diagram

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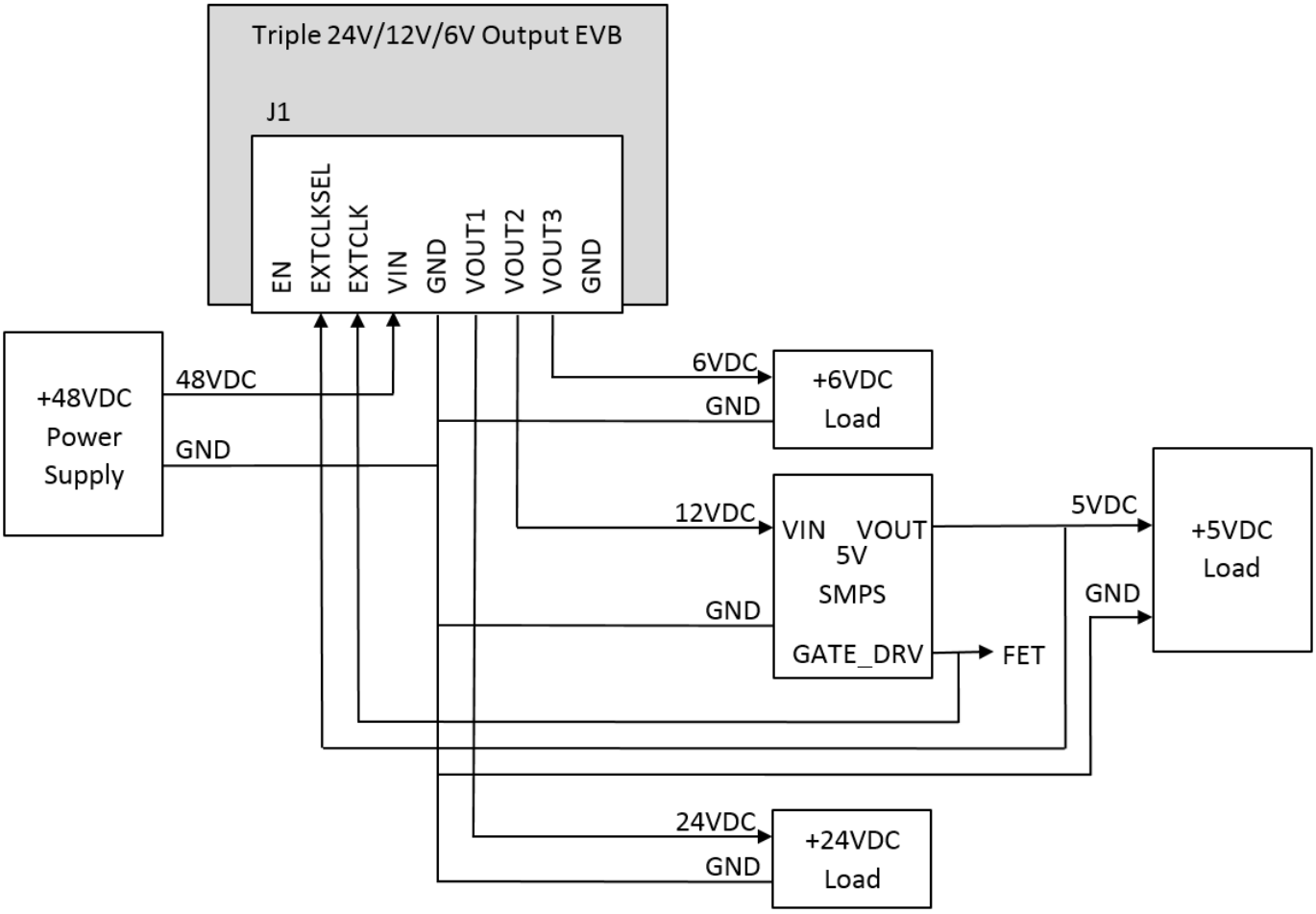

Figure 5: HS200 Triple 24V/12V/6V Output EVB SMPS Wiring Diagram

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Table 3: HS200 Triple 24V/12V/6V Output EVB Connector – J1

Pin No.	Name	Description
1	EN	Device Enable: Input Pin, On-board 100KΩ Pull-Up, 60Vmax 0 = Disable, 1 = Enable
2	EXTCLKSEL	External Clock Sync Enable: Input Pin, Internal 2MΩ Pull-Down, 30Vmax 0 = Internal Clock, 1 = External Clock
3	EXTCLK	External Clock Sync: Input pin, Internal 2MΩ Pull-Down, 30Vmax
4	VIN	+48VDC Input Power Pin
5	GND	Power GND Pin
6	24VOUT	15W +24VDC Output Power Pin
7	12VOUT	10W +12VDC Output Power Pin
8	6VOUT	5W +6VDC Output Power Pin
9	GND	Power GND Pin

Note: Due to board's small size, thermal dissipation is limited. 12VOUT and 6VOUT output power have been reduced to avoid over-temperature shutdown.

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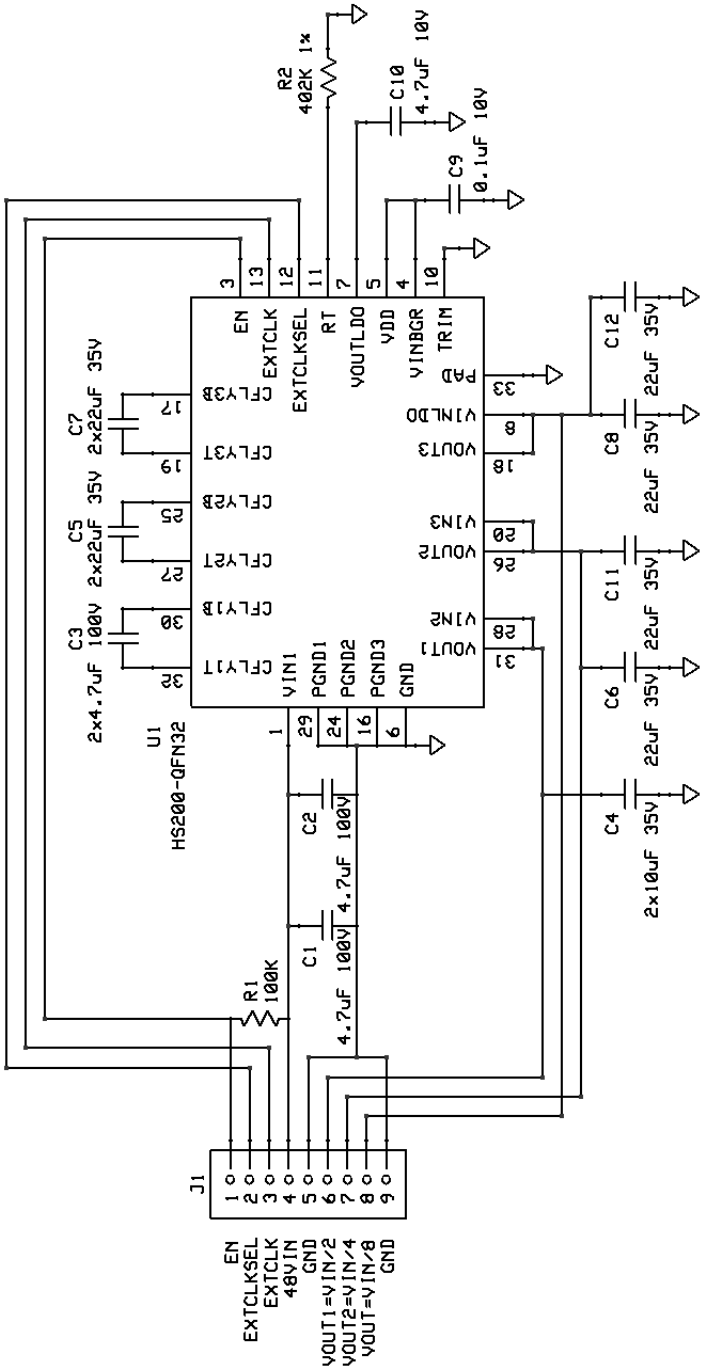

Figure 6: HS200 Triple 24V/12V/6V EVB Output EVB Schematic

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Table 4: HS200 Triple 24V/12V/6V Output EVB Bill of Materials (BOM)

Qty	Ref. No.	Description	Package	Manufacturer
1	C9	CAP, 0.1µF±10%, 10V	CC0603	Murata GRM188R71C104KA01J
1	C10	CAP, 4.7µF±10%, 10V	CC0805	Murata GRM188C81C475KE11J
2	C4x2	CAP, 10µF±10%, 35V	CC0805	Murata GRM21BC8YA106KE11L
8	C5x2, C6, C7x2, C8, C11, C12	CAP, 22µF±10%, 35V	CC0805	TDK C2012X5R1V226M125AC
4	C1, C2, C3x2	CAP, 4.7µF±10%, 100V	CC1206	Murata GRJ32ER71K475KE11L
1	R1	RES, 100KΩ±10%	CC0603	Rohm ESR03EZPJ104
1	R2	RES, 402 KΩ±1%	CC0603	Rohm MCR03ERTF4023
1	U1	IC, HS200, QFN5x5, 32P 0.5	QFN32	Helix Semiconductors
1	J1	CONN, 9P, M, R/A, 0.100	SIP100P9	Hirose A2-9PA-2.54DS(71)

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3 HS200 + 5V Buck Reg. Output EVB

The HS200 + 5V Buck Reg. Output EVB can be operated as a standalone regulated 5V output board (Figure 7) or synchronized with another SMPS (Figure 8).

When the HS200 is providing power to another SMPS, the synchronization feature of the HS200 allows the HS200 MuxCapacitor switching to slow down as the SMPS enters pulse skipping. This operation reduces switching power losses at no-load to light-load conditions. The EXTCLK can be provided by either a FET gate drive signal or a buck regulator's switched output. Both the EXTCLKSEL and EXTCLK inputs accept up to 30V signals.

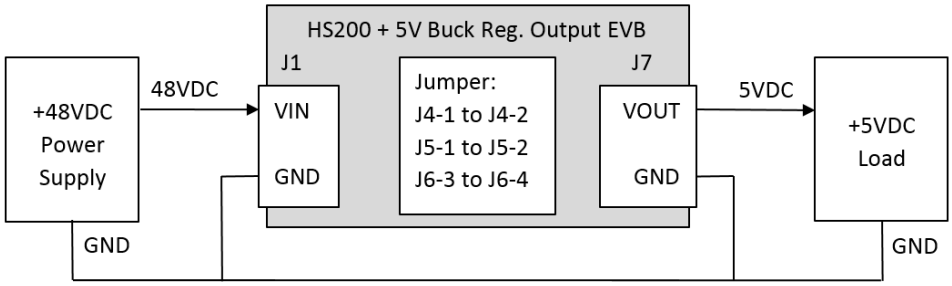

Figure 7: HS200 + 5V Buck Reg. Output EVB Standalone Wiring Diagram

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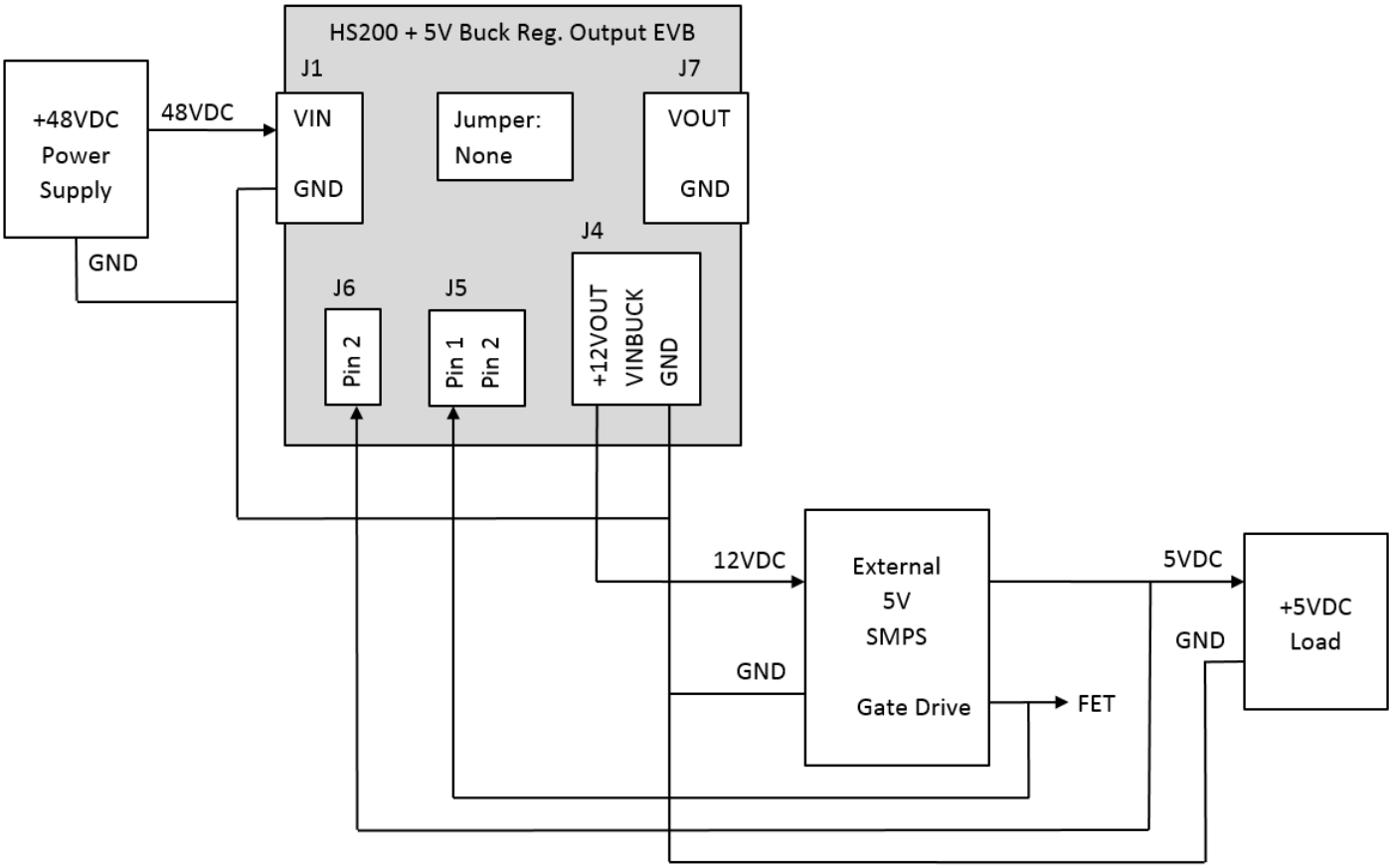

Figure 8: HS200 + 5V Buck Reg. Output EVB using External SMPS Wiring Diagram

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Table 5: HS200 + 5V Buck Reg. Output EVB Connectors

J1 – 48V Input Power

Attach +48V power supply to J1.

Pin No.	Name	Description
1	+48VIN	+48VDC Input Power Pin
2	GND	Power GND Pin

J2 – External Enable (EN) Control

Optional external device enable control signal. Attach to external controller.

Pin No.	Name	Description
1	EN	Device Enable: Input Pin, On-board 100KΩ Pull-Up, 60Vmax 0 = Disable, 1 = Enable
2	GND	GND Pin

J3 – 24V Output Power

Optional +24VDC output.

Pin No.	Name	Description
1	VOUT1	15W +24VDC Output Pin
2	GND	Power GND Pin

J4 – Buck Reg. Input Power

For use with on-board buck regulator, insert jumper to connect pin 1 to pin 2.

For use with external buck regulator, connect pin 1 to buck regulator's input power pin.

Pin No.	Name	Description
1	VOUT2	15W +12VDC output power Pin
2	BUCKIN	On-board buck regulator input power Pin
3	GND	Power GND Pin

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J5 – External Clock

For use with on-board buck regulator, insert jumper to connect pin 1 to pin 2.

For use with external buck regulator, connect pin 1 to buck regulator's FET gate drive signal or inductor switch output. Note: before buck regulator powers up (low output voltage), the HS200 will use its internal clock. Once buck regulator output turns on, the HS200 will synchronize to the buck regulator.

Pin No.	Name	Description
1	EXTCLK	External Clock Sync: Input pin, Internal 2MΩ Pull-Down, 30Vmax
2	GND	GND Pin

J6 – External Clock Selection

Insert jumper from pin 1 to pin 2 to enable external clock input pin.

Insert jumper from pin 3 to pin 4 when using on-board buck regulator.

Insert jumper from pin 5 to pin 6 to use internal HS200 clock.

Pin No.	Name	Description
1	VDD	HS200 VDD output
2	EXTCLKSEL	External Clock Sync Enable: Input Pin, Internal 2MΩ Pull-Down, 30Vmax 0 = Internal Clock, 1 = External Clock
3	VOUT	Buck regulator output
4	EXTCLKSEL	Connected to pin 2, see pin 2 description
5	GND	GND Pin
6	EXTCLKSEL	Connected to pin 2, see pin 2 description.

J7 – 5V Buck Reg. Output Power

Attach +5V load..
Note: Printed circuit board layout noise issue reduces output power. Board change in process.

Pin No.	Name	Description
1	VOUT	On-board buck regulator +5V output pin
2	GND	Power GND Pin

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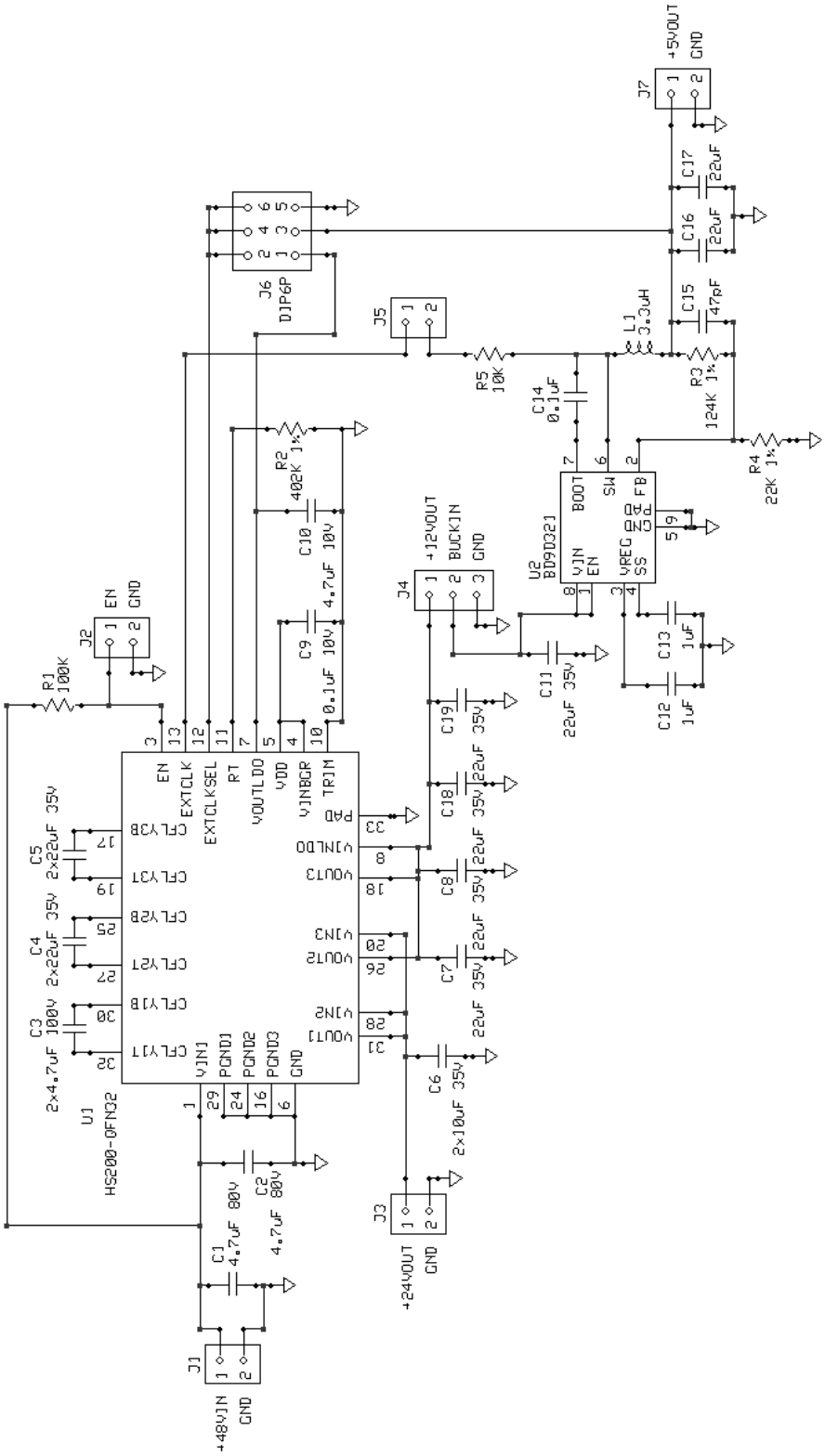

Figure 9 HS200 + 5V Buck Reg. Output EVB Schematic

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Table 6: HS200 + 5V Buck Reg. Output EVB Bill of Materials (BOM)

Qty	Ref. No.	Description	Package	Manufacturer
1	C9	CAP, 0.1µF±10%, 10V	CC0603	Murata GRM188R71C104KA01J
1	C10	CAP, 4.7µF±10%, 10V	CC0805	Murata GRM188C81C475KE11J
2	C6x2	CAP, 10µF±10%, 35V	CC0805	Murata GRM21BC8YA106KE11L
8	C4x2, C5x2, C7, C8, C18, C19	CAP, 22µF±10%, 35V	CC0805	TDK C2012X5R1V226M125AC
4	C1, C2, C3x2	CAP, 4.7µF±10%, 100V	CC1206	Murata GRJ32ER71K475KE11L
1	R1	RES, 100KΩ±10%	CC0603	Rohm ESR03EZPJ104
1	R2	RES, 402KΩ±1%	CC0603	Rohm MCR03ERTF4023
1	U1	IC, HS200, QFN5x5, 32P 0.5	QFN32	Helix Semiconductors
3	J2, J3, J5	CONN, 2P, M, 0.100	SIP2P	Hirose A2-2PA-2.54DSA(71)
1	C15	CAP, 47pF±10%, 50v	CC0603	Murata GRM1885C1H470JA01J
1	C13	CAP, 3300pF±10%, 25v	CC0603	Murata GCM188R71E332KA37D
1	C12	CAP, 1µF±10%, 16V	CC0603	Murata GRM185R61C105KE44J
2	C11, C14	CAP, 0.1µF±10%, 25V	CC0603	Murata GRM188R71E104KA01J
2	C16, C17	CAP, 22µF±10%, 16V	CC1206	Murata GRM31CR61C226KE15K
1	R5	RES, 10KΩ	CC0603	Rohm ESR03EZPJ103
1	R4	RES, 22KΩ±1%	CC0603	Rohm ESR03EZPJ223

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1	R3	RES, 124 KΩ±1%	CC0603	Rohm MCR03ERTF1243
1	L1	IND, 3.3uH, 7.3A	65305	TDK SPM6530T-3R3M
1	U2	IC, BD9D321	HTSOP-J8	Rohm BD9D321EFJ
1	J4	CONN, 3P, M, 0.100	SIP3P	Hirose A2-3PA-2.54DSA(71)
1	J6	CONN, 3x2P, M, 0.100	DIP6P	Hirose A1-6PA-2.54DSA(71)
2	J1, J7	CONN, Terminal Block, 2P	TRMBLK2P	Molex 0398800302

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4 Performance Data

The following MuxCapacitor efficiency data was measured using a Tektronix PM3000 power meter. The figure below shows the test equipment wiring diagram.

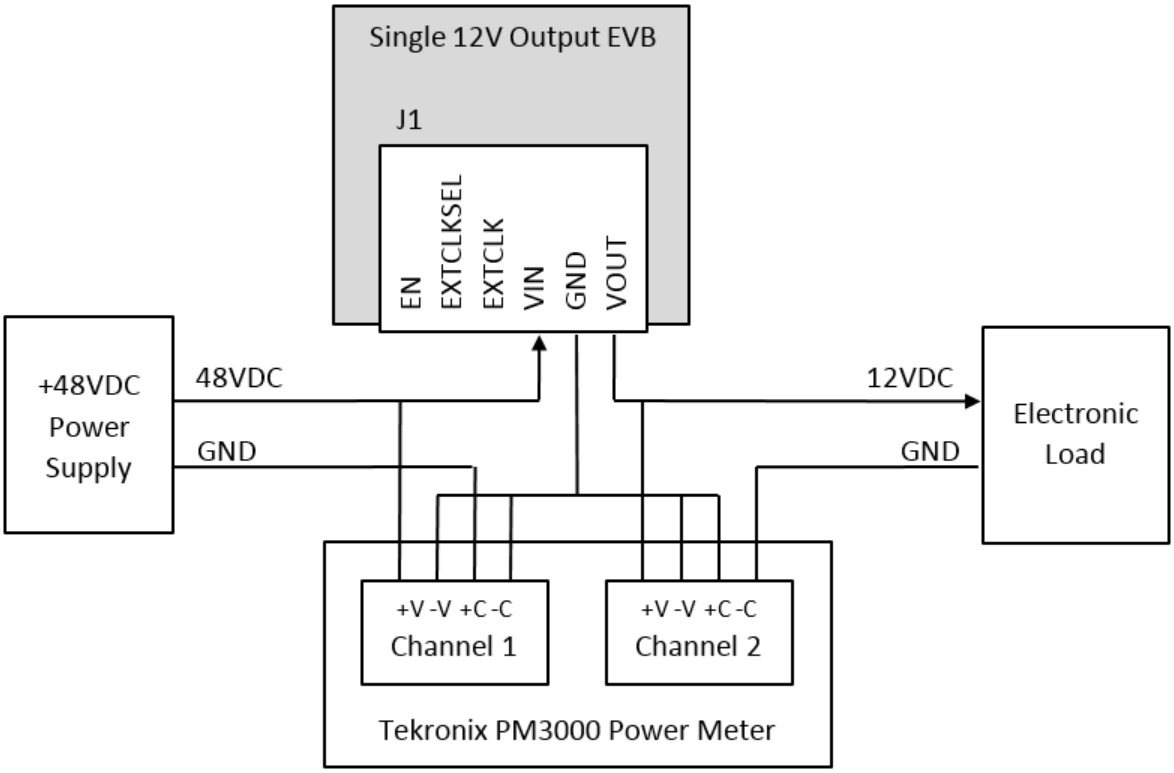

Figure 10: Efficiency Measurement Wiring Diagram

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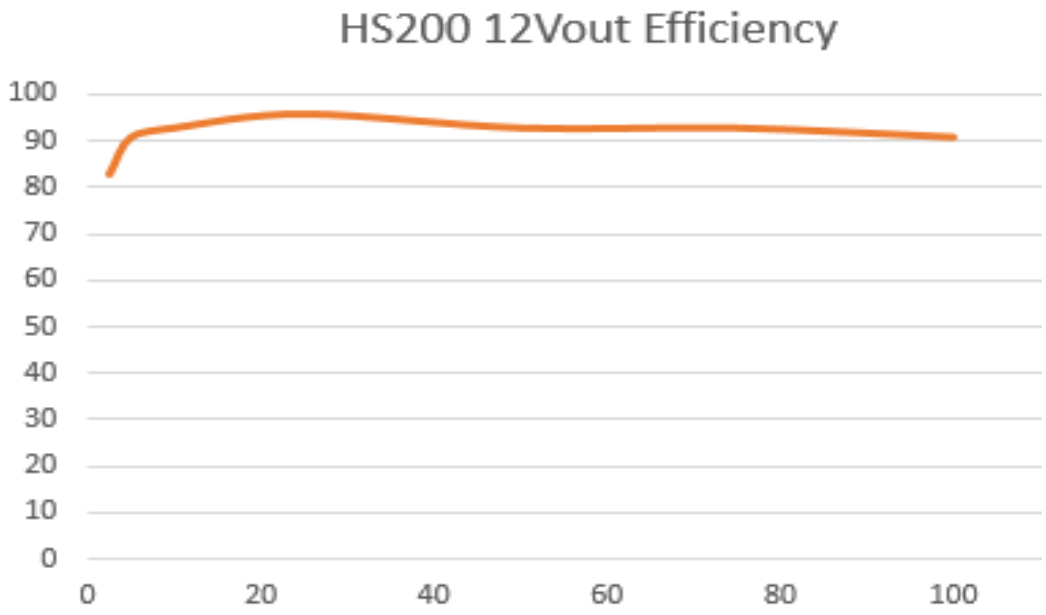

Figure 11: HS200 MuxCapacitor Efficiency

No-Load internal clock (EXTCLKSEL = 0) power disspation < 100mW (48Vin)

No-Load external 100Hz clock (EXTCLKSEL = 1) power disspation < 5mW (48Vin)

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5 Flying Capacitor Value verses Efficiency

The HS200 flying capacitors can be reduced in value for lower output power applications. Lower cost, smaller package size, etc. are tradeoffs that can affect the efficiency performance.

The Flying Capacitor's value is critical to the maximum load operating performance of the MuxCapacitor. If the flying capacitance is too small the efficiency of the MuxCapacitor decreases. Too little capacitance for the required output current effectively behaves as an increase in the impedance of the MuxCapacitor cell.

The effective operating capacitance of ceramic capacitors are subject to a DC Bias derating. As the voltage across the capacitor increases, the capacitor's capacitance value decreases. This DC Bias effect must be considered when operating the capacitor too close to its maximum rated voltage or selecting smaller case sizes.

There are other conditions that must be analyzed for reliable, efficient and safe capacitor operation.

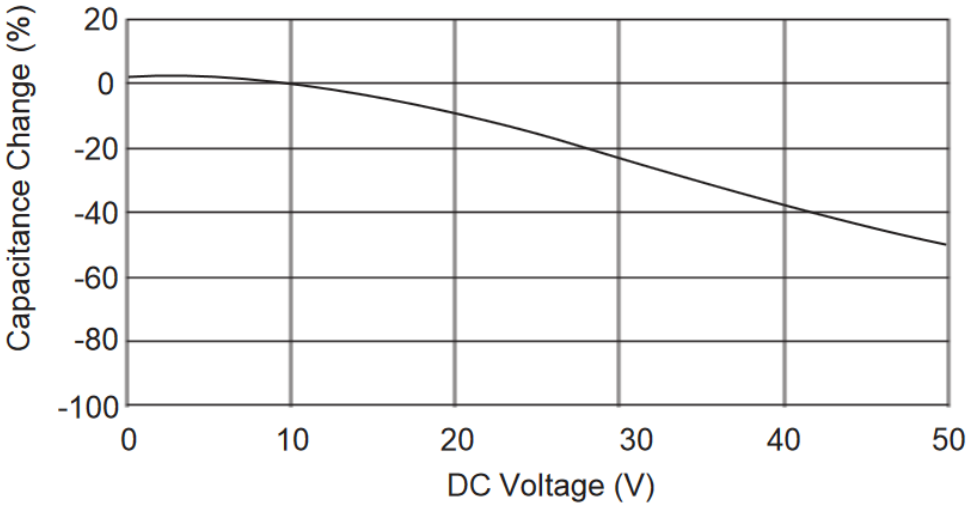

Figure 12: Typical Capacitance verses DC Bias, 50V Device

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Table 7: Revision History

Date	Revision	Description
8.15.17	1	Initial Release
8.30.17	2	Add Fig. 11 Efficiency Data

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